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Overview of the MPEG Reconfigurable Video Coding Initiative

Abstract:

The MPEG Reconfigurable Video Coding initiative, RVC, aims to provide a framework allowing dynamic development, implementation and adoption of standardized video coding solutions with features of higher flexibility and reusability. RVC is motivated by the recognition that standards frameworks need to evolve in order to efficiently support multiple codec configurations and to facilitate innovation in codec design.

Past standards have been instantaneous snapshots of video coding capabilities at a given time. As the process of standardizing a codec can take several years, a codec will be several years out of date by the time standardization is complete and compliant hardware and software hit the market. RVC aims to address this conundrum, by standardizing a framework for codec design, rather than specific codecs themselves. New codecs that are technologically up-to-date can be introduced, and achieve implicit compliance as long as they are developed within the RVC framework.

This talk will provide an overview of the RVC framework, and will introduce its model of computation, which is strongly based on asynchronous data flow (SDF) and the actor-oriented CAL language model, and will focus, in particular, on scheduling algorithms for RVC. Scheduling operations within RVC consists of static (offline) and dynamic (runtime) components. The static schedules are computed at compile time and are collected in a repository for use by the runtime system, which selects entries from the repository and appends them to the ongoing schedule. This talk will summarize techniques to compute RVC schedules in software and with hardware assistance, as well as future research directions.

Bio:

Philip Brisk received his B.S., M.S., and Ph.D. from UCLA in 2002, 2003, and 2006 respectively. From 2006-2009, he was a postdoc at EPFL in Switzerland. He joined the Computer Science and Engineering Department at UCR in 2009. His research interests include reconfigurable computing, design automation and architecture for embedded and application-specific processors, and programmable microfluidic technologies.